ARM Processors

Saurabh, Tushar, Nitesh, Rohan, Paritosh

VIT University

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ARM: Advanced RISC Machines

Origins

- Originated in England in 1984 as Acorn RISC Machines.
- Used mostly for educational systems.
- In 1990, the research section of Acorn separated from the parent company and formed: ARM Ltd.

Figure : England

RISC Machines ?

Basically, a simpler and configurable design for small-scale systems.

- RISC stands for "Reduced Instruction Set Computer"
- Comparision with CISC (Complex Instruction Set Computer)
  - Fixed 32-bit instruction size instead of variable.
  - Larger Register Bank of 32-bit Registers.
  - Easier to prototype and put together.

Why is ARM special

Selling Points

- Best MIPS (Million Instructions Per Second) to Watts ratio
- Best MIPS to $ ratio in the industry.
- The smallest CPU die size.
- Highly Customizable and Flexible.

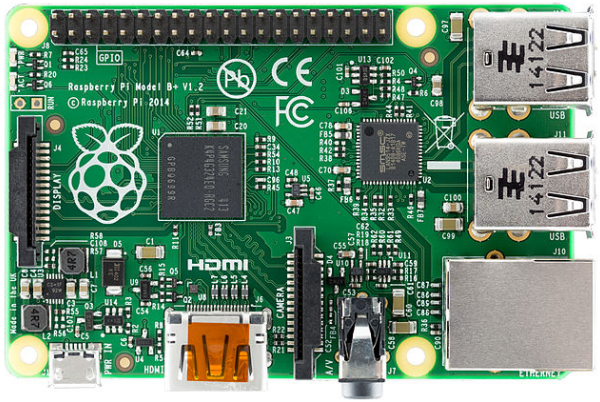


Figure : A Raspberry Pi.

Market Share

The low power consumption of ARM processors has made them very popular: over 50 billion ARM processors have been produced as of 2014.

Figure : ARM-based chips are found in nearly 60 percent of the worlds mobile devices.

Data Sizes and Instruction Sets

- When used in relation to ARM
  - **Halfword** - 16 bits.
  - **Word** - 32 bits.
  - **Doubleword** - 64 bits.
- Most ARMs implement two instruction sets
  - 32 bit ARM instruction set
  - 16 bit Thumb instruction set
- Jazelle-DBX cores can also execute Java bytecode

Processor Modes

- The ARM has seven basic operating modes
- Each mode has its own stack and a different set of registers
- Some operations can only be carried out in a privileged mode

	Mode	Description	
Exception modes	Supervisor (SVC)	**Entered on reset and when a Software Interrupt instruction (SWI) is executed**	Privileged modes
	FIQ	**Entered when a high priority (fast) interrupt is raised**	
	IRQ	**Entered when a low priority (normal) interrupt is raised**	
	Abort	**Used to handle memory access violations**	
	Undef	**Used to handle undefined instructions**	
	System	**Privileged mode using the same registers as User mode**	
	User	**Mode under which most Applications / OS tasks run**	Unprivileged mode

Register Set

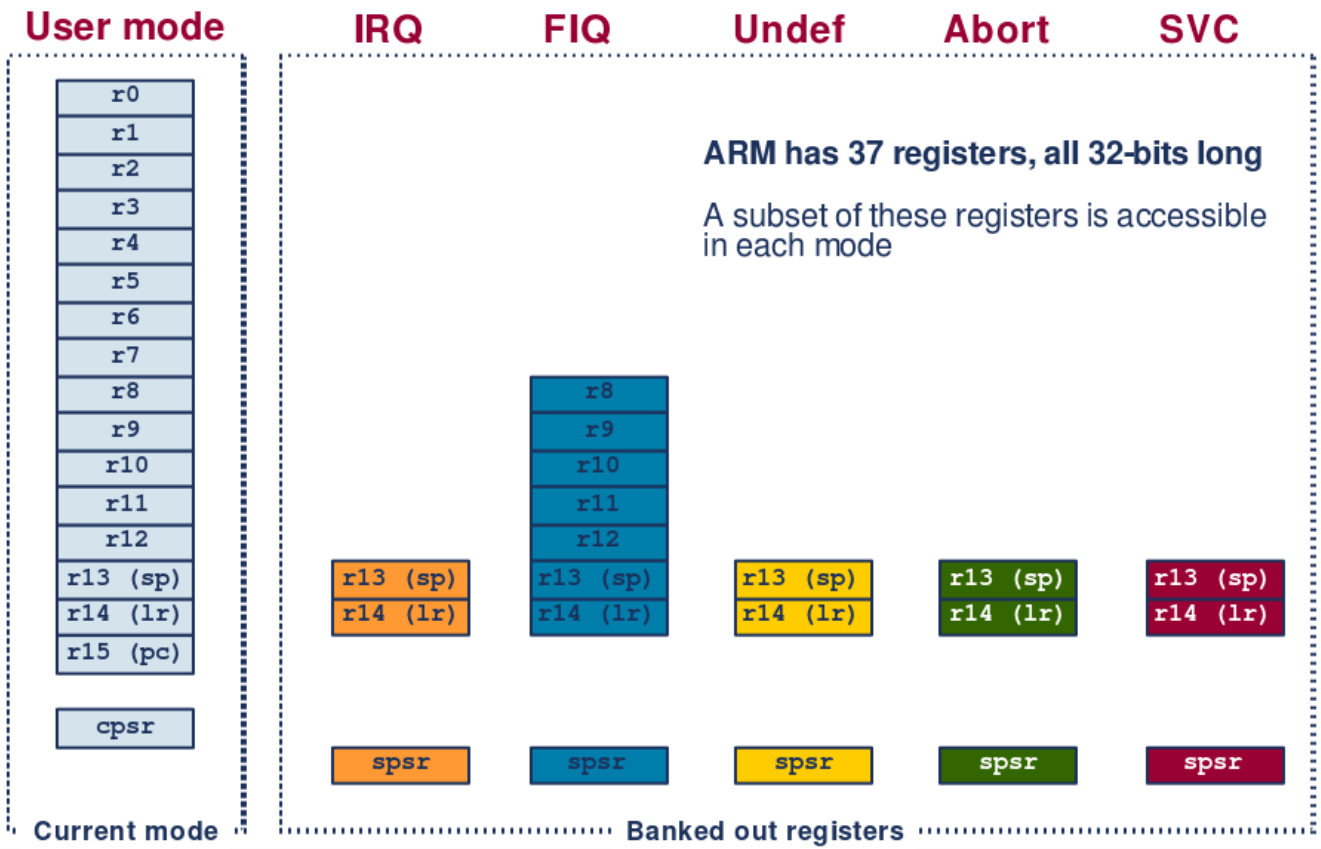


Figure : ARM Register Set.

ARM Instruction Set

All instructions are 32 bit long. Examples

Instruction	**Type**	**Comment**
`sub r0, r1, #5`	data processing	r0 = r1 -5
`B <Label>`	branching	jump (+/- 32MB)
`LDR r0 [r1]`	memory access	load word at address r1 into r0

Table : Examples of ARM instructions

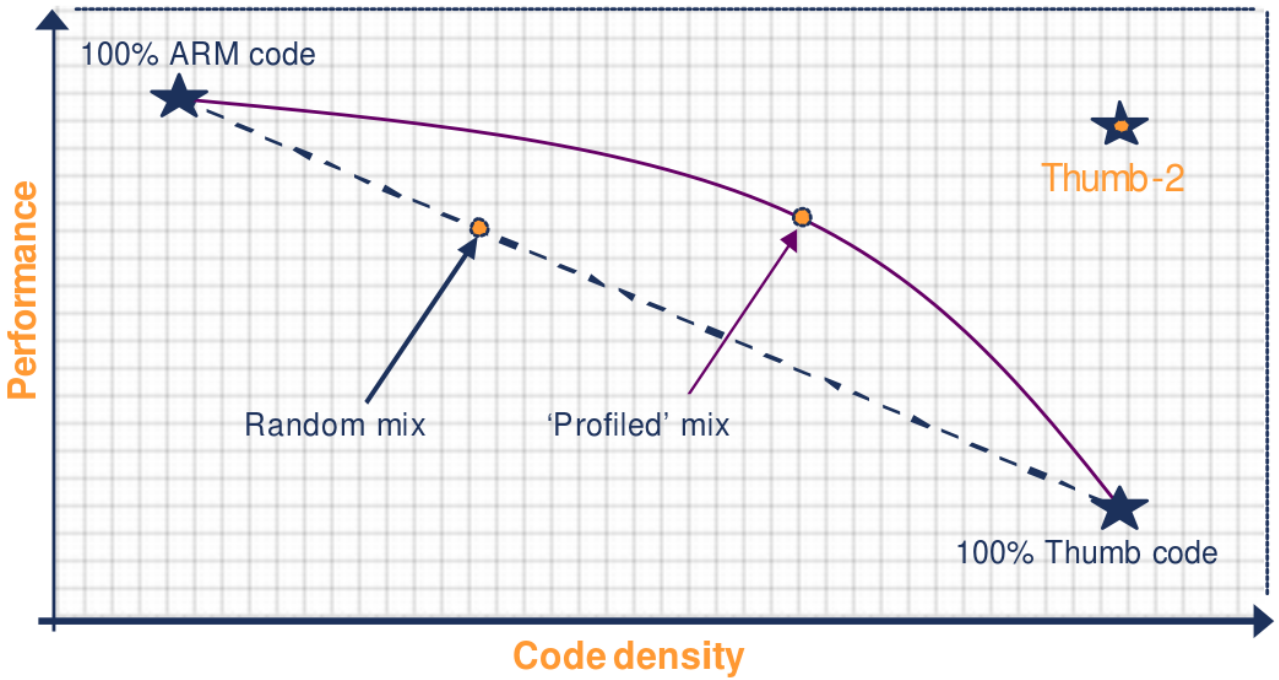
Thumb Instruction Set

- 16 bit instruction set.
  - Optimized for code density from C code (65% ARM code size)
  - Improved performance for narrow memory.
  - Subset of functionality of ARM instruction set.
- Not a "regular" instruction set.
  - Constraints are not generally consistent.
  - Targeted at compiler generation, not hand-coding.

Thumb-2 Instruction Set

- A major extension to the Thumb Instruction Set
  - Adds 32-bit instructions to implement almost all of the ARM functionality
  - Retains the complete 16-bit Thumb instruction set
- Design objective: ARM performance with Thumb code density
  - No switching between states.
  - The Compiler automatically selects mix of 16 and 32 bit instructions.

Comparision



ARM Processors

- ARM1
  - The first ARM processor
  - Used for evaluation systems, mainly a prototype
- ARM2
  - 27 registers, 16 accessible at one time.
  - 8 MHz, 4 Million instructions per second
- ARM3
  - First integrated memory cache.
  - Coprocessor interface added.
  - 25 MHz, 12 Million instructions per second

ARM Processors

- ARM4 & ARM5
  - Never made.
  - Numbering scheme changed due to shift from Acorn to ARM ltd.
- ARM6
  - First to have 32 bit addressing capability.
  - 31 registers, 36,000 transistors
  - 33 MHz, 36 Million instructions per second
- ARM7
  - Functionally identical to ARM6.
  - 26-bit addressing support dropped.
  - 40 MHz, 4 Million instructions per second

ARM Processors

- ARM8
  - 5-stage pipeline.
  - 80 MHz, 80 Million instructions per second
- StrongARM
  - Developed by ARM ltd in conjunction with Digital.
  - 5-stage pipeline.
  - 200 MHz, 230 Million instructions per second
- ARM9
  - 180 MHz, 200 Million instructions per second

ARM Processors

- ARM10
  - Developed by ARM ltd in conjunction with Digital .
  - 300 MHz, 400 Million instructions per second

Cortex

The ARM series were succeeded by the Cortex series of processors

- Cortex-M
- Cortex-R
- Cortex-A (32-bit)
- Cortex-A (64-bit)

The End